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1. A data transfer interface, comprising:

a first bus segment of a first data bus, said first data bus having a first number of data paths;

a second bus segment of said first data bus;

a second data bus having a second number of data paths;

an interface circuit connected between said first and second data buses, wherein said interface circuit is configured to selectively receive data on said first data bus and place said data on said second data bus, said interface circuit being connected to said first data bus between said first and second bus segments of said first data bus for passing data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment.

2. The interface of claim 1, wherein said interface circuit further comprises at least one of a multiplexer and demultiplexer that performs a data rate conversion between said first and second data buses.

3. The interface of claim 2, wherein said interface circuit further comprises a multiplexer and a demultiplexer which perform data rate conversions for data received on said first data bus that is placed on said second data bus and for data received on said second data bus that is placed on said first data bus.

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4. The interface of claim 1, wherein said interface circuit further comprises at least one of a coder and decoder that performs at least one of a data encoding and decoding conversion between said first and second data buses.

5. The interface of claim 1, wherein said interface circuit further comprises a voltage converter that performs a voltage level conversion between said first and second data buses.

6. The interface of claim 1, wherein said first number of data paths is less than said second number of data paths.

7. The interface of claim 1, wherein said second data bus is connected to at least one memory device.

8. The interface of claim 1, wherein said first data bus is connected to a memory controller.

9. The interface of claim 1, wherein said first data bus is connected to a processor.

10. The interface of claim 1, wherein said interface circuit is connected to said first bus segment of said first data bus via a first set of I/O pins and to said second bus segment via a second set of I/O pins, and I/O pins of said first set are connected to respective I/O pins of said second set.

11. The interface of claim 1, wherein said first data bus operates at a first data rate faster than a second data rate at which said second data bus operates.

12. The interface of claim 1, wherein said first data bus operates at a first voltage level less than a second voltage level at which said second data bus operates.

13. The interface of claim 1, wherein said first data bus transmits analog signals.

14. The interface of claim 1, wherein said first data bus transmits digital signals.

15. The interface of claim 1, wherein said first data bus transmits radio-frequency (RF) signals.

16. The interface of claim 1, wherein said interface circuit selects data for receipt from said first data bus according to a selection signal received on a command and address bus.

17. The interface of claim 1, wherein said interface circuit is further configured to selectively receive data on said second data bus and place said data on said first data bus.

18. The interface of claim 17, wherein said interface circuit selects data for receipt from said second data bus according to a selection signal received on a command and address bus.

19. The interface of claim 1, wherein said first data bus is a multidrop bus.

20. The interface of claim 1, wherein said first data bus is a substantially stubless data bus.

21. A memory module, comprising:

at least one memory device;

a data transfer interface connected to a first data bus and to said at least one memory device by a second data bus, said data transfer interface comprising:

a first bus segment of said first data bus, said first data bus having a first number of data paths and said second data bus having a second number of data paths;

a second bus segment of said first data bus;

an interface circuit connected between said first and second data buses, wherein said interface circuit is configured to selectively receive data on said first data bus and place said data on said second data bus, said interface circuit being connected to said first data bus between said first and second bus segments of said first data bus for

passing data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment.

22. The memory module of claim 21, wherein said interface circuit further comprises at least one of a multiplexer and demultiplexer that performs a data rate conversion between said first and second data buses.

23. The memory module of claim 22, wherein said interface circuit further comprises a multiplexer and a demultiplexer which perform data rate conversions for data received on said first data bus that is placed on said second data bus and for data received on said second data bus that is placed on said first data bus.

24. The memory module of claim 21, wherein said interface circuit further comprises at least one of a coder and decoder that performs at least one of a data encoding and decoding conversion between said first and second data buses.

25. The memory module of claim 21, wherein said interface circuit further comprises a voltage converter that performs a voltage level conversion between said first and second data buses.

26. The memory module of claim 21, wherein said first number of data paths is less than said second number of data paths.

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27. The memory module of claim 21, wherein said first data bus is connected to a memory controller.

28. The memory module of claim 21, wherein said first data bus is connected to a processor.

29. The memory module of claim 21, wherein said interface circuit is connected to said first bus segment of said first data bus via a first set of I/O pins and to said second bus segment via a second set of I/O pins, and I/O pins of said first set are connected to respective I/O pins of said second set.

30. The memory module of claim 21, wherein said first data bus operates at a first data rate faster than a second data rate at which said second data bus operates.

31. The memory module of claim 21, wherein said first data bus operates at a first voltage level less than a second voltage level at which said second data bus operates.

32. The memory module of claim 21, wherein said first data bus transmits analog signals.

33. The memory module of claim 21, wherein said first data bus transmits digital signals.

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34. The memory module of claim 21, wherein said first data bus transmits radio-frequency (RF) signals.

35. The memory module of claim 21, wherein said interface circuit selects data for receipt from said first data bus according to a selection signal received on a command and address bus.

36. The memory module of claim 21, wherein said interface circuit is further configured to selectively receive data on said second data bus and place said data on said first data bus.

37. The memory module of claim 36, wherein said interface circuit selects data for receipt from said second data bus according to a selection signal received on a command and address bus.

38. The memory module of claim 21, wherein said first data bus is a multidrop bus.

39. The memory module of claim 21, wherein said first data bus is a substantially stubless data bus.

40. A data exchange system, comprising:

a first data bus having at least first and second bus segments;

a controller connected to place data on and receive data from said first data bus;

a processor connected to said controller via a second bus, and

a data transfer interface circuit connected to said first data bus and to a third data bus, wherein said interface circuit is configured to selectively receive data on said first data bus and place said data on said third data bus, said interface circuit being connected to said first data bus between said first and second bus segments of said first data bus for passing data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment.

41. A data exchange system, comprising:

a first data bus having at least first and second bus segments;

a processor connected to place data on and receive data from said first data bus; and

a data transfer interface circuit connected to said first data bus and to a second data bus, wherein said interface circuit is configured to selectively receive data on said first data bus and place said data on said second data bus, said interface circuit being connected to said first data bus between said first and second bus segments of said first data bus for passing data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment.

42. A data transmission system comprising:

at least one processor;

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at least one plurality of data devices which transmit and receive data over M-bit data paths;

a respective interface device associated with each of said plurality of data devices; and

a bus system having N data paths, where N is less than M, for exchanging data between said processor and said data devices, which loops through each of said interface devices.

43. A data transmission system comprising;

a processor;

a least one memory subsystem connected to said processor; and

a bus which loops through each of a controller and at least one memory subsystem interface circuit of said at least one memory subsystem;

whereby said memory subsystem interface circuit couples at least one memory device to said bus, said memory subsystem interface circuit comprising a circuit for receiving data from said bus and converting it to data which can be processed by said at least one memory device and for receiving data from said at least one memory device and converting it to data which can be transmitted over said bus.

44. A processor system as in claim 43, wherein said controller resides on a same printed circuit board as said processor.

45. A processor system as in claim 43, wherein said controller is integrated into said processor.

46. A method of data communication between devices in an electronic circuit, comprising:

connecting a first port of an interface circuit having first and second sets of I/O pins to respective first and second segments of a first data bus that operates at a first data rate;

connecting a second port of said interface circuit to a second data bus that operates at a second data rate;

receiving and transmitting data on said first data bus using said first and second sets of I/O pins of said first port;

receiving and transmitting data on said second data bus using said second port;

selectively converting data received from one of said first and second data buses at one of said first and second ports for use on the other of said first and second data buses; and

passing data on said first data bus through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment.

47. A method as in claim 46, wherein said selectively converting data includes using a selection signal to determine whether to convert for use on the other of said first and second data buses.

48. A method as in claim 47, wherein said selective conversion of data is performed when said interface circuit is selected for operation by said selection signal.

49. A method as in claim 47, wherein said selective conversion of data is not performed when said interface circuit is not selected for operation by said selection signal.

50. A method as in claim 46, wherein said first data rate is faster than said second data rate.

51. A method as in claim 46, further comprising converting received data between said first data rate of said first data bus and said second data rate of said second data bus.

52. A method as in claim 46, further comprising converting received data between a first encoding of said first data bus and a second encoding of said second data bus.

53. A method as in claim 46, further comprising converting received data between a first voltage level of said first data bus to a second voltage level of said second data bus.

54. A method as in claim 53, wherein said first voltage level is less than said second voltage level.

55. A method as in claim 46, wherein said first data bus connects to said first and second sets of I/O pins of said first port using a first bus width different from a second bus width used to connect said second port to said second data bus.

56. A method as in claim 55, wherein said first bus width is less than said second bus width.

57. A method as in claim 46, wherein devices of a first technology communicate with said interface circuit using said first data bus and devices of a second technology communicate with said interface circuit using said second data bus.

58. A method as in claim 57, wherein said devices of said first technology include at least one processor.

59. A method as in claim 57, wherein said devices of said second technology include at least one memory device.

60. A method as in claim 46, wherein said looping data bus is a multi-drop bus.

61. A method as in claim 46, wherein said looping data bus is a substantially stubless data bus.